

APPLICATION FOR UNITED STATES LETTERS PATENT

FOR

COMPOSITE SOURCE FOLLOWER

Inventors: Sateh M. Jalaleddine
Suharli Tedja

Prepared by: Mendelsohn & Associates, P.C.
1515 Market Street, Suite 715
Philadelphia, Pennsylvania 19102
(215) 557-6657
Customer No. 22186

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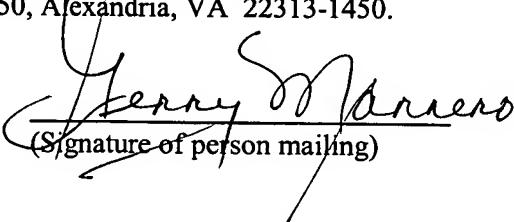
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COMPOSITE SOURCE FOLLOWER

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present invention relates to electronics, and, in particular, to source follower circuits.

Description of the Related Art

10 Source followers are used to buffer signals and provide low output impedance to drive resistive loads. Traditional source followers have load drive capability limited to the quiescent current in the buffer. In addition, traditional source followers require too much power for many applications.

15 To reduce power dissipation (and area) required to reach a given output resistance, a super source follower configuration is sometimes used. See P.R. Gray, P.J. Hurst, S.H. Lewis, and R.G. Meyer, Analysis and Design of Analog Integrated Circuits, 4th ed., John Wiley & Sons, Inc., New York, 2001, pp. 213-215, the teachings of which are incorporated herein by reference. Unfortunately, the PMOS boost of this solution is too slow for many applications.

20 U.S. Patent Publication No. 2002/0175761 A1 (Bach et al.), the teachings of which are incorporated herein by reference, describes a PMOS version of a folded source follower. Unfortunately, this PMOS super source follower is also too slow for many applications.

SUMMARY OF THE INVENTION

25 Problems in the prior art are addressed in accordance with the principles of the present invention by a composite source follower with enhanced drive. According to certain embodiments of the present invention, the drain current of a source follower (e.g., an NMOS source follower) is sensed, e.g., with a folded cascode device. The sensed current from the folded cascode is multiplied to the output load using a current mirror device of the same type as the source follower.

BRIEF DESCRIPTION OF THE DRAWINGS

30 Other aspects, features, and advantages of the present invention will become more fully apparent from the following detailed description, the appended claims, and the accompanying drawings in which like reference numerals identify similar or identical elements.

Fig. 1 shows a schematic circuit diagram of a composite source follower, according to one embodiment of the present invention.

DETAILED DESCRIPTION

Reference herein to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment can be included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment, nor are separate or alternative embodiments necessarily mutually exclusive of other embodiments.

Fig. 1 shows a schematic circuit diagram of a composite source follower 100, according to one embodiment of the present invention. At a functional level, composite source follower 100 comprises a current source configured to provide a (relatively) constant current to the rest of the circuit, a source follower configured to receive an input signal VIN, a folded cascode device connected to sense the drain current of the source follower, and a current mirror device connected to multiply the sensed drain current for application to an output load connected at the source follower output VOUT.

At the device level, composite source follower 100 comprises five MOS transistors M0-M4. In the implementation shown in Fig. 1, transistors M0-M2 are NMOS devices, and transistors M3-M4 are PMOS devices. In an alternative implementation, M0-M2 may be PMOS devices and M3-M4 may be NMOS devices.

As shown in Fig. 1, the source of transistor M3 is connected to the supply voltage Vdd, the gate of M3 is connected to bias voltage vbp1, and the drain of M3 is connected to (1) the source of transistor M4 and (2) the drain of transistor M2.

The gate of transistor M4 is connected to bias voltage vbp2, and the drain of M4 is connected to (1) the drain of transistor M1, (2) the gate of M1, and (3) the gate of transistor M0.

The source of transistor M1 is connected to ground.

The gate of transistor M2 is connected to the input voltage VIN, and the source of M2 is connected to (1) the drain of transistor M0 and (2) the output voltage VOUT.

The source of transistor M0 is connected to ground.

Transistor M3 functions as a (relatively) constant current source for composite source follower 100, with the current from M3 being divided between transistor M4 and transistor M2. The gate bias voltage vbp1 is preferably selected to ensure that transistor M3 stays in saturation for all expected operations of composite source follower 100.

Transistors M0 and M2 are configured as a source follower. In particular, with the input VIN applied to the gate of M2, and both the source of M2 and the drain of M0 connected to the output VOUT, the voltage at output VOUT will be proportional to (i.e., will follow) the voltage applied at input VIN.

Transistors M0 and M1 are configured as current mirrors, with the current through M0 mirrored by (i.e., proportional to) the current through M1, and vice versa. In the implementation of Fig. 1, M0 is

three times the size of M1. As such, the current through M0 will be approximately three times as large as the current through M1. In other implementations, this ratio of 3:1 may be different. Depending on the requirements of the particular circuit application, the magnitude of the ratio may be limited by the stability of the circuit, e.g., to a maximum of about 4:1.

5 With an appropriate gate bias voltage v_{bp2} applied, transistor M4 functions as a folded cascode device that senses the drain current of transistor M2. The sensed current is then multiplied by the current mirror. M4 acts as a current buffer of gain 1 that prevents the current mirror from being overloaded.

10 When an input voltage signal is applied at input V_{IN} , a portion of the signal goes to the output V_{OUT} via the gate-to-source of M2, while another portion of the signal goes to the output V_{OUT} via the gate-to-drain of M2, through M4, and through the gate-to-drain of M0. This second signal path functions as a signal feed-back path in composite source follower 100. The effect of this feed-back signal is to reduce the voltage at output V_{OUT} even more than the voltage reduction from the first signal path (i.e., the gate-to-source of M2). As a result, the voltage at output V_{OUT} will be a smaller fraction of the voltage at input V_{IN} than if the circuitry included only the source follower combination of transistors M0 and M2. As such, composite source follower 100 can be used as a buffer for applications in which the output V_{OUT} is to be connected to drive relatively low-impedance loads.

15 Another way to look at the operations of composite source follower 100 is to analyze the current flow. The current I_3 from current source M3 is divided into a current I_2 to transistor M2 and a current I_4 to transistor M4, where $I_3=I_2+I_4$. The current I_2 is itself divided into a current I_{out} at V_{OUT} and a current I_0 through transistor M0, where $I_2=I_{out}+I_0$.

20 An increase in the voltage applied at input V_{IN} causes the current I_2 through M2 to increase. As a result, the current I_4 through transistor M4 (and therefore through transistor M1) decreases. This decrease in current through M1 is mirrored by a decrease in current through M0, where the decrease in current is multiplied by a factor of 3. This amplified decrease in the current I_0 through M0 causes an increased fraction of the current I_2 to flow to V_{OUT} as current I_{out} .

25 The result is an increase in the overall transconductance of composite source follower 100 as compared to the source follower configuration of transistors M2 and M0 alone. In particular, the overall transconductance of composite source follower 100 is $(1+Loop_gain)$, where $Loop_gain$ is a function of the ratio of the transistors in the current mirror (e.g., 3 for the implementation of Fig. 1). Thus, composite source follower 100 provides a four-fold increase in transconductance as compared to the source follower of M2 and M0 alone.

30 As used in the following claims, the term “channel nodes” refer to the source and drain of a transistor.

The invention has been described in the context of a composite source follower comprising a constant current source, a source follower, a folded cascode device that senses the drain current of the source follower, and a current mirror that multiplies the sensed drain current, each of which has been described as being implemented in composite source follower 100 of Fig. 1 with specific types of devices. Those skilled in the art will understand that the invention can also be implemented using different devices. For example, the particular sizes of the individual devices might also change depending on the particular application. As mentioned previously, the NMOS devices may be replaced with PMOS devices, and vice versa. Furthermore, devices of suitable technologies other than MOS can be used, such as bipolar technology. For bipolar implementations, for example, the terms drain, source, and gate used in both this specification and in the following claims will be understood to refer to the collector, emitter, and base, respectively, of bipolar devices. Moreover, each of the constant current source, the source follower, the folded cascode device, and the current mirror might be able to be implemented using different configurations of devices to achieve similar or analogous functions.

Although the present invention is preferably implemented as part of a single integrated circuit, it may also be implemented using discrete devices.

It will be further understood that various changes in the details, materials, and arrangements of the parts which have been described and illustrated in order to explain the nature of this invention may be made by those skilled in the art without departing from the scope of the invention as expressed in the following claims.